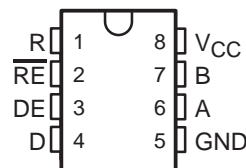


SN65ALS176, SN75ALS176, SN75ALS176A, SN75ALS176B DIFFERENTIAL BUS TRANSCEIVERS

SLLS040G – AUGUST 1987 – REVISED DECEMBER 1999

- Meet or Exceed the Requirements of TIA/EIA-422-B, TIA/EIA-485-A, and ITU Recommendations V.11 and X.27
- Operate at Data Rates up to 35 MBaud
- Four Skew Limits Available:
 - SN65ALS176 . . . 15 ns
 - SN75ALS176 . . . 10 ns
 - SN75ALS176A . . . 7.5 ns
 - SN75ALS176B . . . 5 ns
- Designed for Multipoint Transmission on Long Bus Lines in Noisy Environments
- Low Supply-Current Requirements . . . 30 mA Max
- Wide Positive and Negative Input/Output Bus-Voltage Ranges
- Thermal Shutdown Protection
- Driver Positive and Negative Current Limiting
- Receiver Input Hysteresis
- Glitch-Free Power-Up and Power-Down Protection
- Receiver Open-Circuit Fail-Safe Design

D OR P PACKAGE
(TOP VIEW)



description

The SN65ALS176 and SN75ALS176 series differential bus transceivers are designed for bidirectional data communication on multipoint bus transmission lines. They are designed for balanced transmission lines and meet TIA/EIA-422-B, TIA/EIA-485-A, and ITU Recommendations V.11 and X.27.

The SN65ALS176 and SN75ALS176 series combine a 3-state, differential line driver and a differential input line receiver, both of which operate from a single 5-V power supply. The driver and receiver have active-high and active-low enables, respectively, that can be connected together externally to function as a direction control. The driver differential outputs and the receiver differential inputs are connected internally to form a differential input/output (I/O) bus port that is designed to offer minimum loading to the bus when the driver is disabled or $V_{CC} = 0$. This port features wide positive and negative common-mode voltage ranges, making the device suitable for party-line applications.

The SN65ALS176 is characterized for operation from -40°C to 85°C , and the SN75ALS176 series is characterized for operation from 0°C to 70°C .



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS
INSTRUMENTS**

POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

Copyright © 1999, Texas Instruments Incorporated

SN65ALS176, SN75ALS176, SN75ALS176A, SN75ALS176B DIFFERENTIAL BUS TRANSCEIVERS

SLLS040G – AUGUST 1987 – REVISED DECEMBER 1999

AVAILABLE OPTIONS

T _A	t _{sk(lim)} †	PACKAGED DEVICES	
		SMALL OUTLINE (D)‡	PLASTIC DIP (P)
0°C to 70°C	10	SN75ALS176D	SN75ALS176P
	7.5	SN75ALS176AD	SN75ALS176AP
	5	SN75ALS176BD	SN75ALS176BP
-40°C to 85°C	15	SN65ALS176D	SN65ALS176P

† t_{sk(lim)} This is the maximum range that the driver or receiver delay times vary over temperature, V_{CC}, and process (device to device).

‡ The D package is available taped and reeled. Add the suffix R to the device type (e.g., SN75ALS176DR).

Function Tables

DRIVER

INPUT D	ENABLE DE	OUTPUTS	
		A	B
H	H	H	L
L	H	L	H
X	L	Z	Z

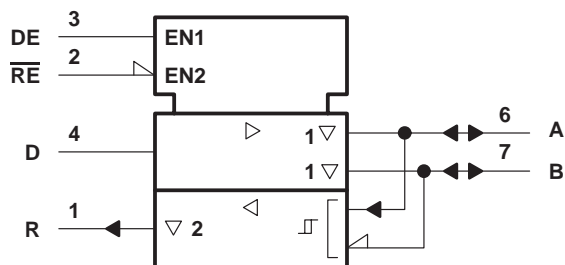
H = high level, L = low level, X = irrelevant,
Z = high impedance

RECEIVER

DIFFERENTIAL INPUTS A-B	ENABLE \overline{RE}	OUTPUT R
V _{ID} ≥ 0.2 V	L	H
-0.2 V < V _{ID} < 0.2 V	L	?
V _{ID} ≤ -0.2 V	L	L
X	H	Z
Inputs open	L	H

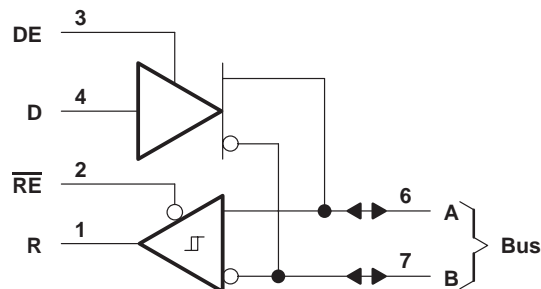
H = high level, L = low level, X = irrelevant,
Z = high impedance

logic symbol§



§ This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

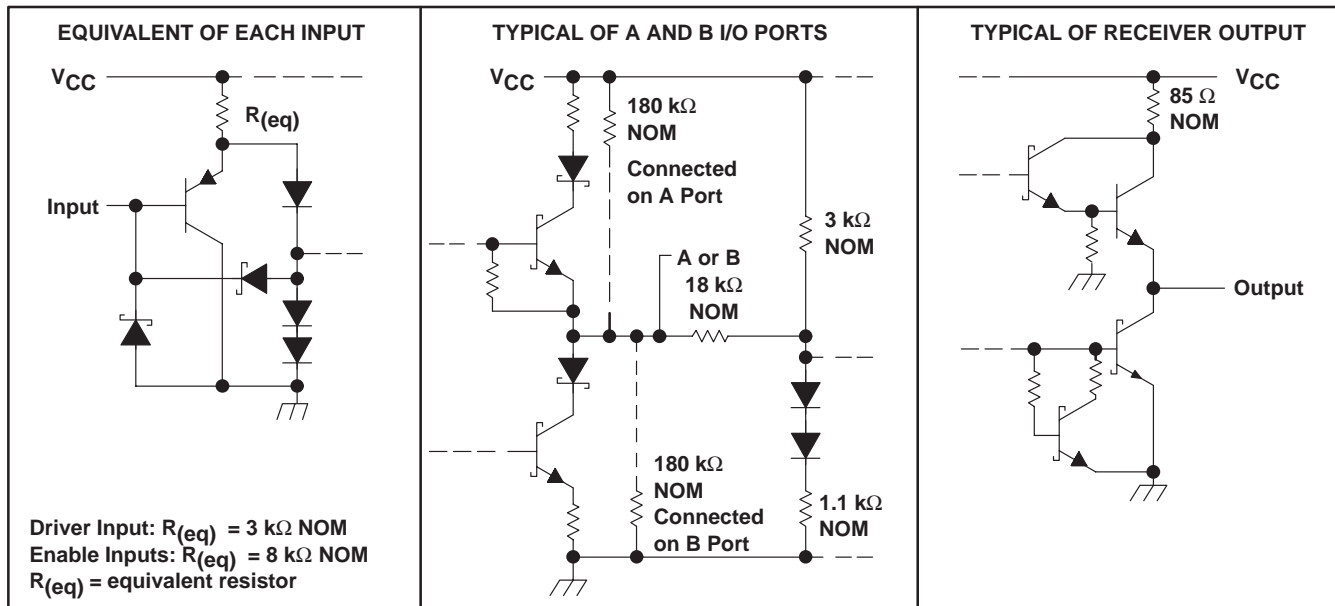
logic diagram (positive logic)



SN65ALS176, SN75ALS176, SN75ALS176A, SN75ALS176B DIFFERENTIAL BUS TRANSCEIVERS

SLLS040G – AUGUST 1987 – REVISED DECEMBER 1999

schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1)	7 V
Voltage range at any bus terminal	-7 V to 12 V
Enable input voltage, V_I	5.5 V
Package thermal impedance, θ_{JA} (see Note 2):	
D package	197°C/W
P package	104°C/W
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C
Storage temperature range, T_{Stg}	-65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. All voltage values, except differential I/O bus voltage, are with respect to network ground terminal.
 2. The package thermal impedance is calculated in accordance with JESD 51.

SN65ALS176, SN75ALS176, SN75ALS176A, SN75ALS176B DIFFERENTIAL BUS TRANSCEIVERS

SLLS040G – AUGUST 1987 – REVISED DECEMBER 1999

recommended operating conditions (unless otherwise noted)

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
Input voltage at any bus terminal (separately or common mode), V_I or V_{IC}		12			V
		-7			
High-level input voltage, V_{IH}	D, DE, and \overline{RE}	2			V
Low-level input voltage, V_{IL}	D, DE, and \overline{RE}	0.8			V
Differential input voltage, V_{ID} (see Note 3)		± 12			V
High-level output current, I_{OH}	Driver	-60			mA
	Receiver	-400			μA
Low-level output current, I_{OL}	Driver	60			mA
	Receiver	8			
Operating free-air temperature, T_A	SN65ALS176	-40	85		$^{\circ}C$
	SN75ALS176 series	0	70		

NOTE 3: Differential input/output bus voltage is measured at the noninverting terminal A with respect to the inverting terminal B.



SN65ALS176, SN75ALS176, SN75ALS176A, SN75ALS176B DIFFERENTIAL BUS TRANSCEIVERS

SLLS040G – AUGUST 1987 – REVISED DECEMBER 1999

DRIVER SECTION

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IK}	Input clamp voltage	$I_I = -18 \text{ mA}$				-1.5	V
V_O	Output voltage	$I_O = 0$		0		6	V
$ V_{OD1} $	Differential output voltage	$I_O = 0$		1.5		6	V
$ V_{OD2} $	Differential output voltage	$R_L = 100 \Omega$,	See Figure 1	$1/2 V_{OD1}$ or 2V^{\S}			V
		$R_L = 54 \Omega$,	See Figure 1	1.5	2.5	5	V
V_{OD3}	Differential output voltage	$V_{test} = -7 \text{ V to } 12 \text{ V}$,	See Figure 2	1.5		5	V
$\Delta V_{OD} $	Change in magnitude of differential output voltage¶	$R_L = 54 \Omega \text{ or } 100 \Omega$, See Figure 1				± 0.2	V
V_{OC}	Common-mode output voltage					3 -1	V
$\Delta V_{OC} $	Change in magnitude of common-mode output voltage¶					± 0.2	V
I_O	Output current	Outputs disabled, See Note 4	$V_O = 12 \text{ V}$			1	mA
			$V_O = -7 \text{ V}$			-0.8	
I_{IH}	High-level input current	$V_I = 2.4 \text{ V}$				20	μA
I_{IL}	Low-level input current	$V_I = 0.4 \text{ V}$				-400	μA
I_{OS}	Short-circuit output current#	$V_O = -4 \text{ V}$	SN65ALS176			-250	mA
		$V_O = -6 \text{ V}$	SN75ALS176				
		$V_O = 0$				-150	
		$V_O = V_{CC}$				250	
		$V_O = 8 \text{ V}$					
I_{CC}	Supply current	No load	Outputs enabled		23	30	mA
			Outputs disabled		19	26	

† The power-off measurement in TIA/EIA-422-B applies to disabled outputs only and is not applied to combined inputs and outputs.

‡ All typical values are at $V_{CC} = 5 \text{ V}$ and $T_A = 25^\circ\text{C}$.

§ The minimum V_{OD2} with a 100- Ω load is either $1/2 V_{OD1}$ or 2 V, whichever is greater.

¶ $\Delta |V_{OD}|$ and $\Delta |V_{OC}|$ are the changes in magnitude of V_{OD} and V_{OC} , respectively, that occur when the input is changed from one logic state to the other.

Duration of the short circuit should not exceed one second for this test.

NOTE 4: This applies for power on and power off. Refer to TIA/EIA-485-A for exact conditions. The TIA/EIA-422-B limit does not apply for a combined driver and receiver terminal.

SN65ALS176, SN75ALS176, SN75ALS176A, SN75ALS176B

DIFFERENTIAL BUS TRANSCEIVERS

SLLS040G – AUGUST 1987 – REVISED DECEMBER 1999

switching characteristics over recommended ranges of supply voltage and operating free-air temperature range (unless otherwise noted)

SN65ALS176

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
$t_d(OD)$	Differential output delay time	$R_L = 54 \Omega$, $C_L = 50 \text{ pF}$, See Figure 3			15	ns
$t_{sk(p)}$	Pulse skew‡	$R_L = 54 \Omega$, $C_L = 50 \text{ pF}$, See Figure 3		0	2	ns
$t_{sk(lim)}$	Pulse skew§				15	
$t_t(OD)$	Differential output transition time	$R_L = 54 \Omega$, $C_L = 50 \text{ pF}$, See Figure 3		8		ns
t_{PZH}	Output enable time to high level	$R_L = 110 \Omega$, $C_L = 50 \text{ pF}$, See Figure 4			80	ns
t_{PZL}	Output enable time to low level	$R_L = 110 \Omega$, $C_L = 50 \text{ pF}$, See Figure 5			30	ns
t_{PHZ}	Output disable time from high level	$R_L = 110 \Omega$, $C_L = 50 \text{ pF}$, See Figure 4			50	ns
t_{PLZ}	Output disable time from low level	$R_L = 110 \Omega$, $C_L = 50 \text{ pF}$, See Figure 5			30	ns

† All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$.

‡ Pulse skew is defined as the $|t_{PLH} - t_{PHL}|$ of each channel of the same device.

§ Skew limit is the maximum difference in propagation delay times between any two channels of any two devices.

SN75ALS176, SN75ALS176A, SN75ALS176B

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT			
$t_d(OD)$	Differential output delay time	$R_L = 54 \Omega$, $C_L = 50 \text{ pF}$, See Figure 3			'ALS176	3	8	13	ns
					'ALS176A	4	7	11.5	
					'ALS176B	5	8	10	
$t_{sk(p)}$	Pulse skew‡	$R_L = 54 \Omega$, $C_L = 50 \text{ pF}$, See Figure 3		0	2	ns			
$t_{sk(lim)}$	Pulse skew§	$R_L = 54 \Omega$, $C_L = 50 \text{ pF}$, See Figure 3			'ALS176			10	ns
					'ALS176A			7.5	
					'ALS176B			5	
$t_t(OD)$	Differential output transition time	$R_L = 54 \Omega$, $C_L = 50 \text{ pF}$, See Figure 3		8		ns			
t_{PZH}	Output enable time to high level	$R_L = 110 \Omega$, $C_L = 50 \text{ pF}$, See Figure 4		23	50	ns			
t_{PZL}	Output enable time to low level	$R_L = 110 \Omega$, $C_L = 50 \text{ pF}$, See Figure 5		14	20	ns			
t_{PHZ}	Output disable time from high level	$R_L = 110 \Omega$, $C_L = 50 \text{ pF}$, See Figure 4		20	35	ns			
t_{PLZ}	Output disable time from low level	$R_L = 110 \Omega$, $C_L = 50 \text{ pF}$, See Figure 5		8	17	ns			

† All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$.

‡ Pulse skew is defined as the $|t_{PLH} - t_{PHL}|$ of each channel of the same device.

§ Skew limit is the maximum difference in propagation delay times between any two channels of any two devices.

SYMBOL EQUIVALENTS

DATA-SHEET PARAMETER	TIA/EIA-422-B	TIA/EIA-485-A
V_O	V_{Oa}, V_{Ob}	V_{Oa}, V_{Ob}
$ V_{OD1} $	V_O	V_O
$ V_{OD2} $	$V_t (R_L = 100 \Omega)$	$V_t (R_L = 54 \Omega)$
$ V_{OD3} $	None	V_t (test termination measurement 2)
$\Delta V_{OD} $	$ V_t - \bar{V}_t $	$ V_t - \bar{V}_t $
V_{OC}	$ V_{Os} $	$ V_{Os} $
$\Delta V_{OC} $	$ V_{Os} - \bar{V}_{Os} $	$ V_{Os} - \bar{V}_{Os} $
I_{OS}	$ I_{sa} , I_{sb} $	None
I_O	$ I_{xa} , I_{xb} $	I_{ia}, I_{ib}



SN65ALS176, SN75ALS176, SN75ALS176A, SN75ALS176B DIFFERENTIAL BUS TRANSCEIVERS

SLLS040G – AUGUST 1987 – REVISED DECEMBER 1999

RECEIVER SECTION

electrical characteristics over recommended ranges of common-mode input voltage, supply voltage, and operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V _{IT+}	Positive-going input threshold voltage	V _O = 2.7 V,	I _O = -0.4 mA			0.2	V
V _{IT-}	Negative-going input threshold voltage	V _O = 0.5 V,	I _O = 8 mA	-0.2‡			V
V _{hys}	Hysteresis voltage (V _{IT+} - V _{IT-})				60		mV
V _{IK}	Enable-input clamp voltage	I _I = -18 mA				-1.5	V
V _{OH}	High-level output voltage	V _{ID} = 200 mV, See Figure 6	I _{OH} = -400 μA,		2.7		V
V _{OL}	Low-level output voltage	V _{ID} = -200 mV, See Figure 6	I _{OL} = 8 mA,			0.45	V
I _{OZ}	High-impedance-state output current	V _O = 0.4 V to 2.4 V				±20	μA
V _I	Line input current	Other input = 0 V, See Note 4	V _I = 12 V			1	mA
			V _I = -7 V			-0.8	
I _{IH}	High-level-enable input current	V _{IH} = 2.7 V				20	μA
I _{IL}	Low-level-enable input current	V _{IL} = 0.4 V				-100	μA
r _I	Input resistance			12	20		kΩ
I _{OS}	Short-circuit output current	V _{ID} = 200 mV,	V _O = 0	-15		-85	mA
I _{CC}	Supply current	No load	Outputs enabled		23	30	mA
			Outputs disabled		19	26	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

‡ The algebraic convention, in which the less positive (more negative) limit is designated minimum, is used in this data sheet for common-mode input voltage and threshold voltage levels only.

NOTE 5: This applies for power on and power off. Refer to TIA/EIA-485-A for exact conditions.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature range (unless otherwise noted)

SN65ALS176

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
t _{pd}	Propagation time	V _{ID} = -1.5 V to 1.5 V, See Figure 7	C _L = 15 pF,			25	ns
t _{sk(p)}	Pulse skew§					0	2
t _{sk(lim)}	Pulse skew¶	R _L = 54 Ω, See Figure 3	C _L = 50 pF,			15	ns
t _{PZH}	Output enable time to high level	C _L = 15 pF,	See Figure 8		11	18	ns
t _{PZL}	Output enable time to low level				11	18	ns
t _{PHZ}	Output disable time from high level					50	ns
t _{PLZ}	Output disable time from low level					30	ns

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

§ Pulse skew is defined as the |t_{PLH} - t_{PHL}| of each channel of the same device.

¶ Skew limit is the maximum difference in propagation delay times between any two channels of any two devices.



SN65ALS176, SN75ALS176, SN75ALS176A, SN75ALS176B DIFFERENTIAL BUS TRANSCEIVERS

SLLS040G – AUGUST 1987 – REVISED DECEMBER 1999

switching characteristics over recommended ranges of supply voltage and operating free-air temperature range (unless otherwise noted) (continued)

SN75ALS176, SN75ALS176A, SN75ALS176B

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
t _{pd}	Propagation time	'ALS176	V _{ID} = -1.5 V to 1.5 V, C _L = 15 pF, See Figure 7	9	14	19	ns
		'ALS176A		10.5	14	18	
		'ALS176B		11.5	13	16.5	
t _{sk(p)}	Pulse skew‡			0	2		ns
t _{sk(lim)}	Pulse skew§	'ALS176	R _L = 54 Ω, See Figure 3		10		ns
		'ALS176A			7.5		
		'ALS176B			5		
t _{pZH}	Output enable time to high level			7	14		ns
t _{pZL}	Output enable time to low level			20	35		ns
t _{pHZ}	Output disable time from high level			20	35		ns
t _{pLZ}	Output disable time from low level			8	17		ns

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

‡ Pulse skew is defined as the |t_{pLH} - t_{pHL}| of each channel of the same device.

§ Skew limit is the maximum difference in propagation delay times between any two channels of any two devices.

PARAMETER MEASUREMENT INFORMATION

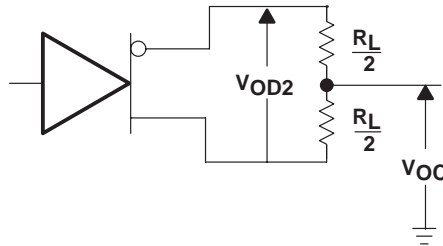


Figure 1. Driver V_{OD2} and V_{OC}

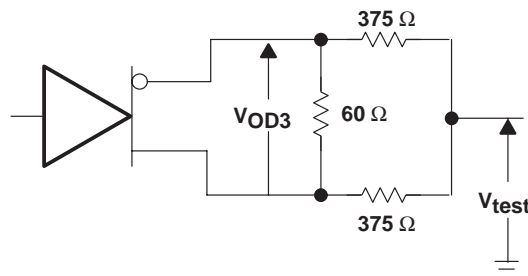
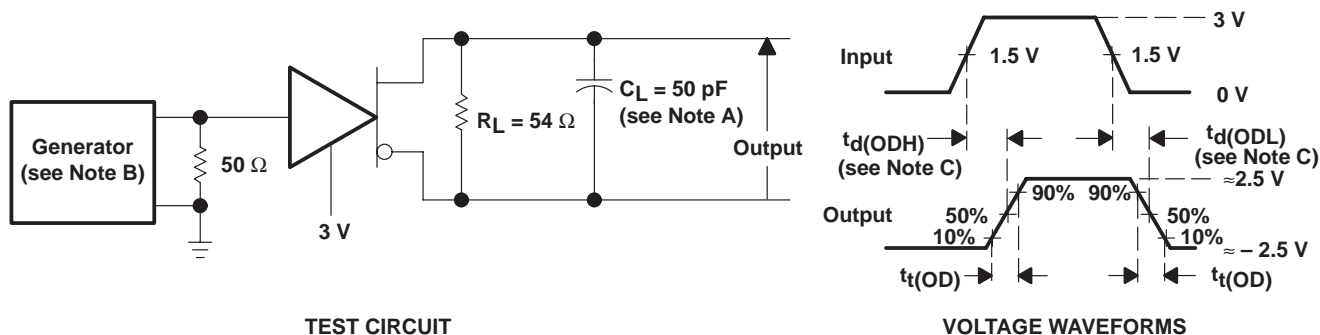


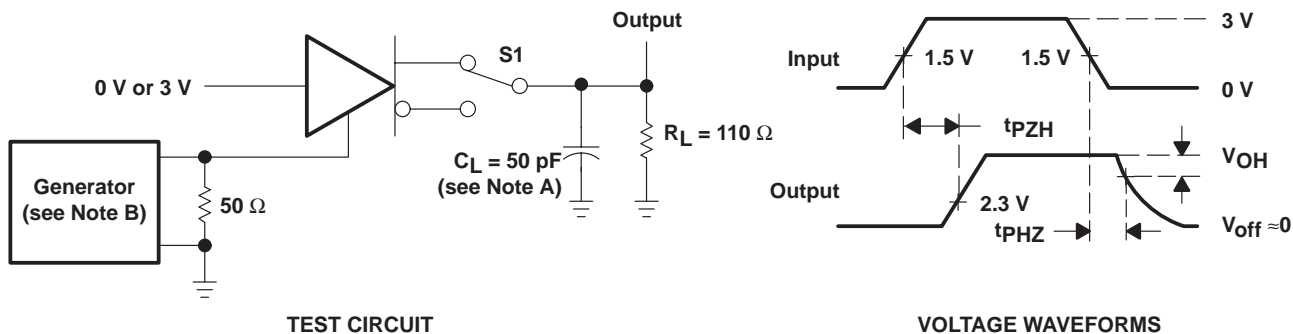
Figure 2. Driver V_{OD3}

PARAMETER MEASUREMENT INFORMATION



- NOTES: A. C_L includes probe and jig capacitance.
 B. The input pulse is supplied by a generator having the following characteristics: PRR \leq 1 MHz, 50% duty cycle, $t_r \leq$ 6 ns, $t_f \leq$ 6 ns, $Z_O = 50 \Omega$.
 C. $t_d(OD) = t_d(ODH)$ or $t_d(ODL)$

Figure 3. Driver Test Circuit and Voltage Waveforms



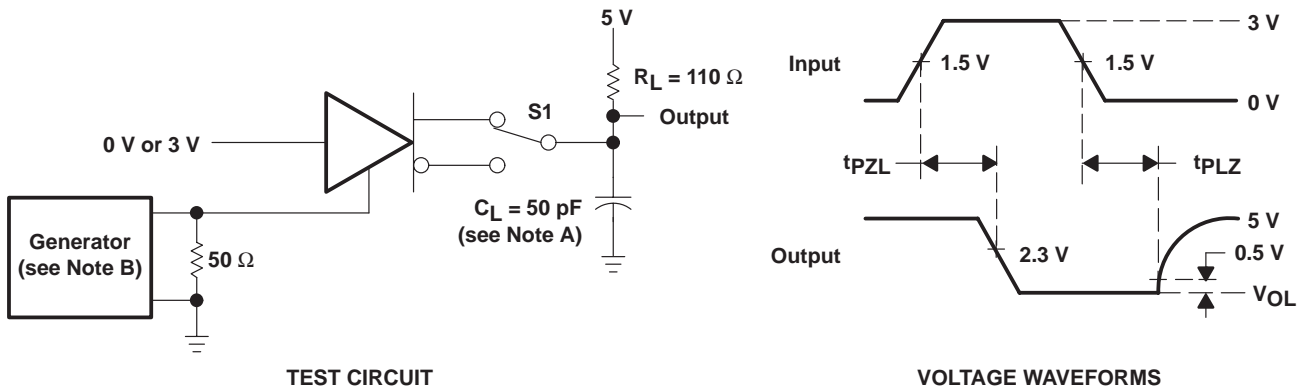
- NOTES: A. C_L includes probe and jig capacitance.
 B. The input pulse is supplied by a generator having the following characteristics: PRR \leq 1 MHz, 50% duty cycle, $t_r \leq$ 6 ns, $t_f \leq$ 6 ns, $Z_O = 50 \Omega$.

Figure 4. Driver Test Circuit and Voltage Waveforms

SN65ALS176, SN75ALS176, SN75ALS176A, SN75ALS176B DIFFERENTIAL BUS TRANSCEIVERS

SLLS040G – AUGUST 1987 – REVISED DECEMBER 1999

PARAMETER MEASUREMENT INFORMATION



- NOTES: A. C_L includes probe and jig capacitance.
 B. The input pulse is supplied by a generator having the following characteristics: $PRR \leq 1$ MHz, 50% duty cycle, $t_r \leq 6$ ns, $t_f \leq 6$ ns, $Z_O = 50 \Omega$.

Figure 5. Driver Test Circuit and Voltage Waveforms

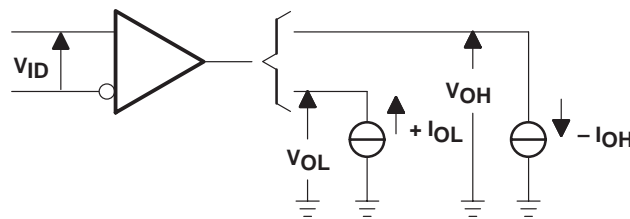
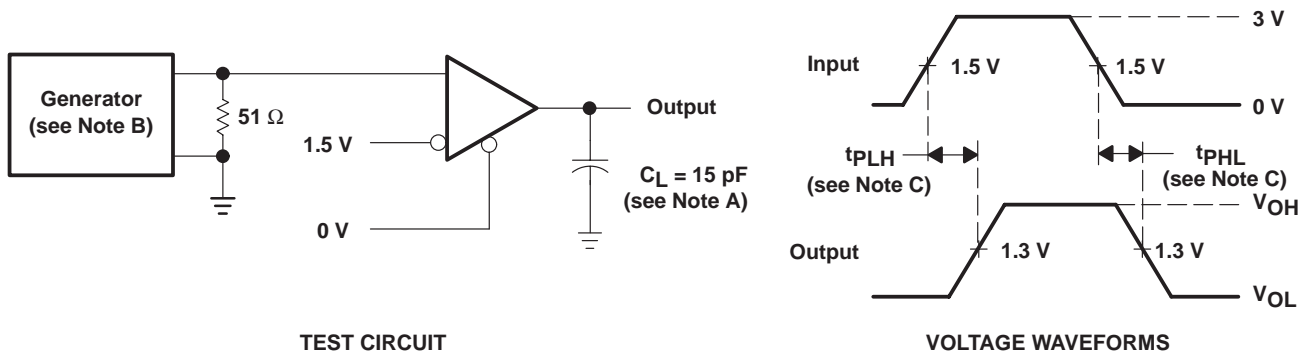


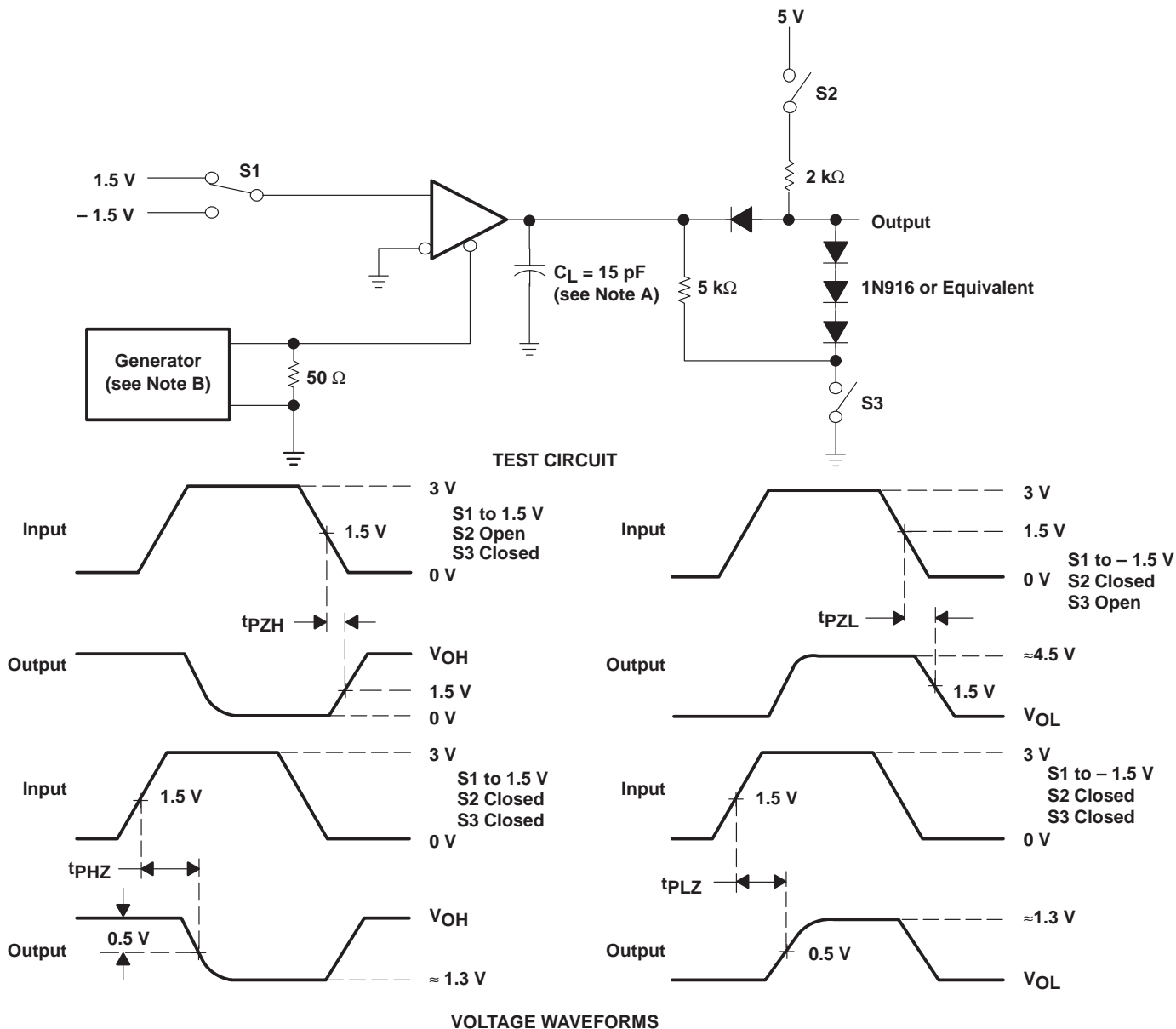
Figure 6. Receiver V_{OH} and V_{OL} Test Circuit



- NOTES: A. C_L includes probe and jig capacitance.
 B. The input pulse is supplied by a generator having the following characteristics: $PRR \leq 1$ MHz, 50% duty cycle, $t_r \leq 6$ ns, $t_f \leq 6$ ns, $Z_O = 50 \Omega$.
 C. $t_{pd} = t_{PLH}$ or t_{PHL}

Figure 7. Receiver Test Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_L includes probe and jig capacitance.
B. The input pulse is supplied by a generator having the following characteristics: PRR \leq 1 MHz, 50% duty cycle, $t_r \leq$ 6 ns, $t_f \leq$ 6 ns, $Z_0 = 50 \Omega$.

Figure 8. Receiver Test Circuit and Voltage Waveforms

SN65ALS176, SN75ALS176, SN75ALS176A, SN75ALS176B DIFFERENTIAL BUS TRANSCEIVERS

SLLS040G – AUGUST 1987 – REVISED DECEMBER 1999

TYPICAL CHARACTERISTICS†

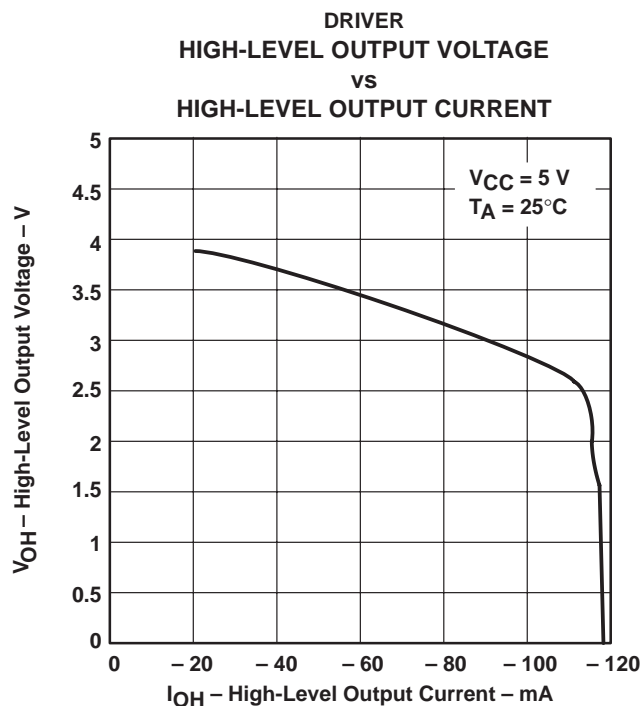


Figure 9

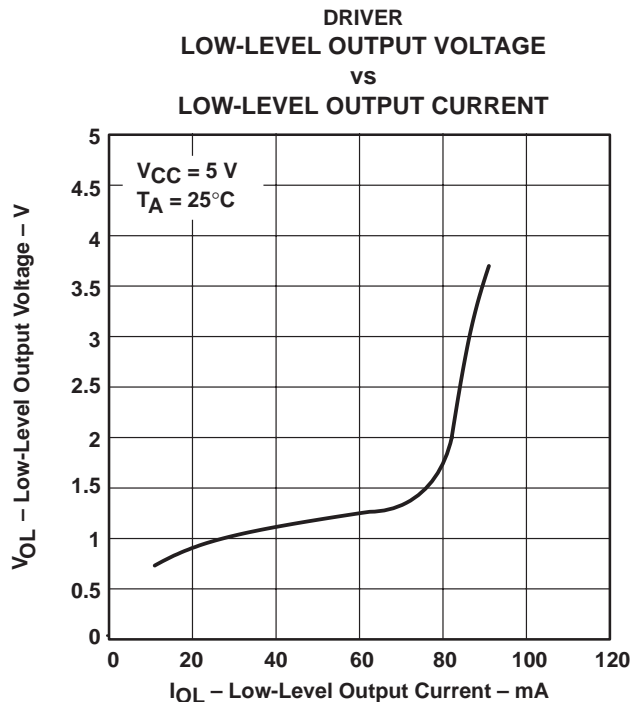


Figure 10

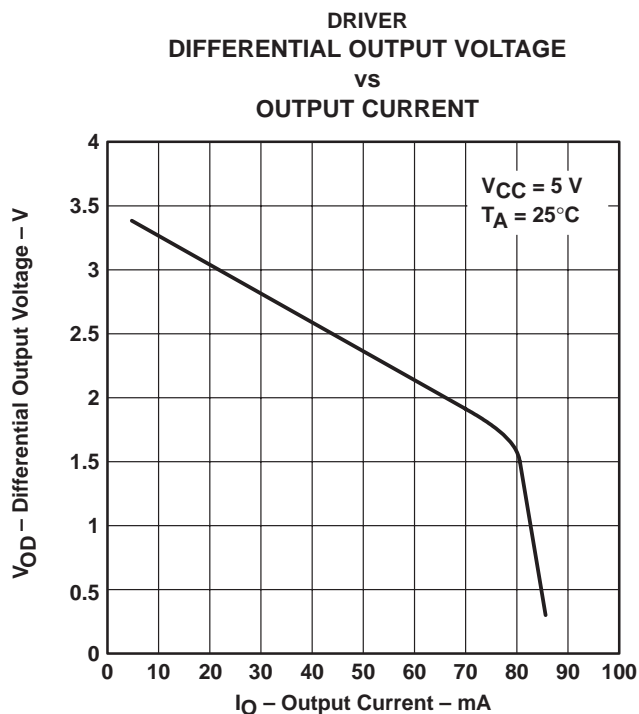
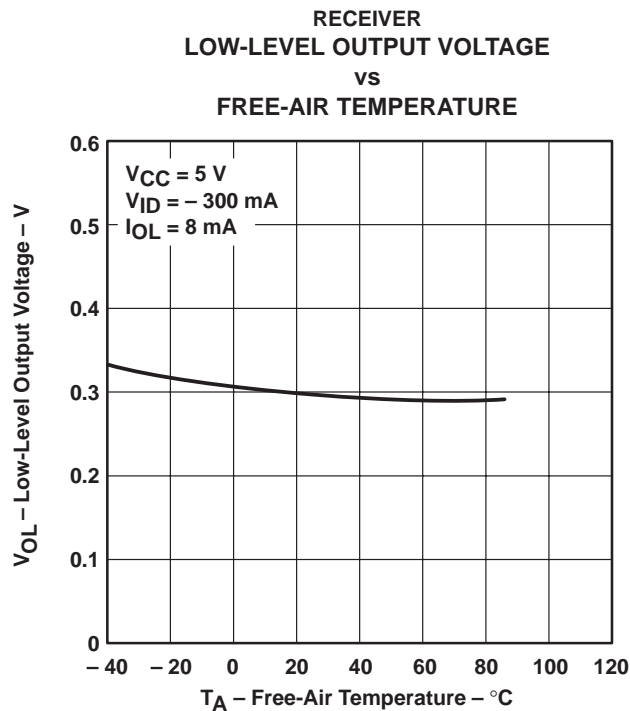
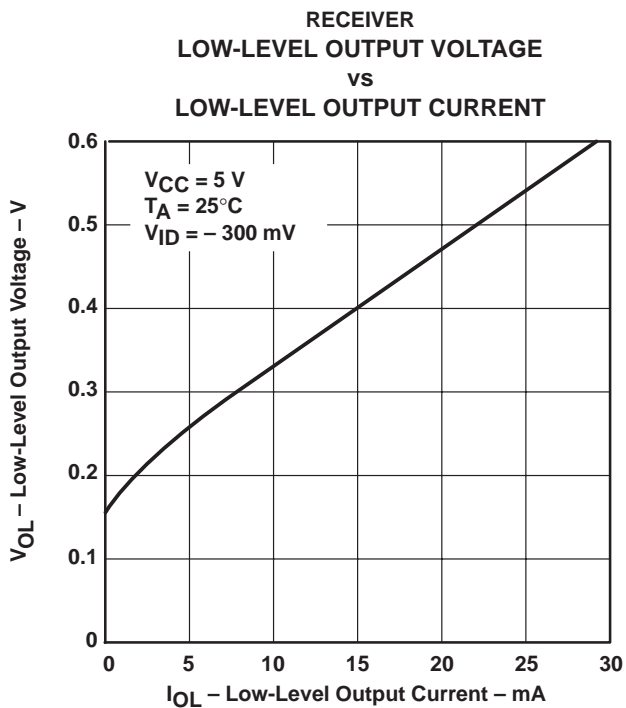
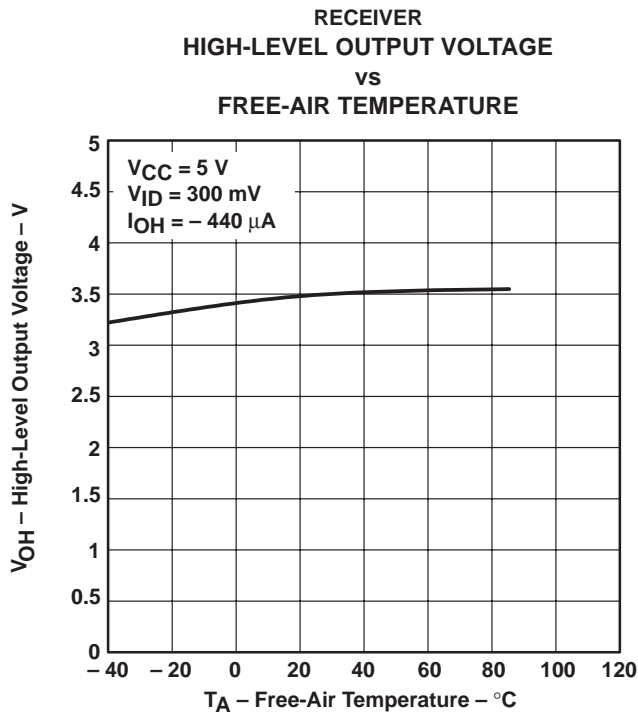
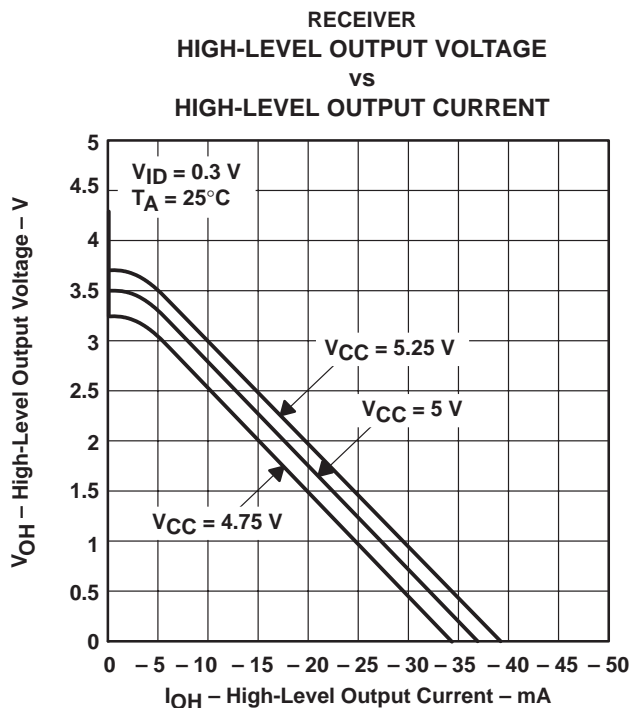


Figure 11

† Operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied.

TYPICAL CHARACTERISTICS†



† Operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied.

SN65ALS176, SN75ALS176, SN75ALS176A, SN75ALS176B DIFFERENTIAL BUS TRANSCEIVERS

SLLS040G – AUGUST 1987 – REVISED DECEMBER 1999

TYPICAL CHARACTERISTICS†

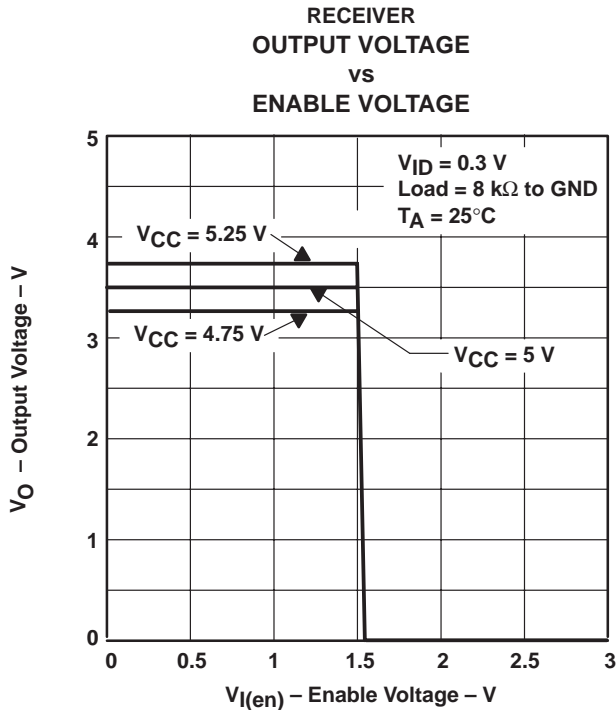


Figure 16

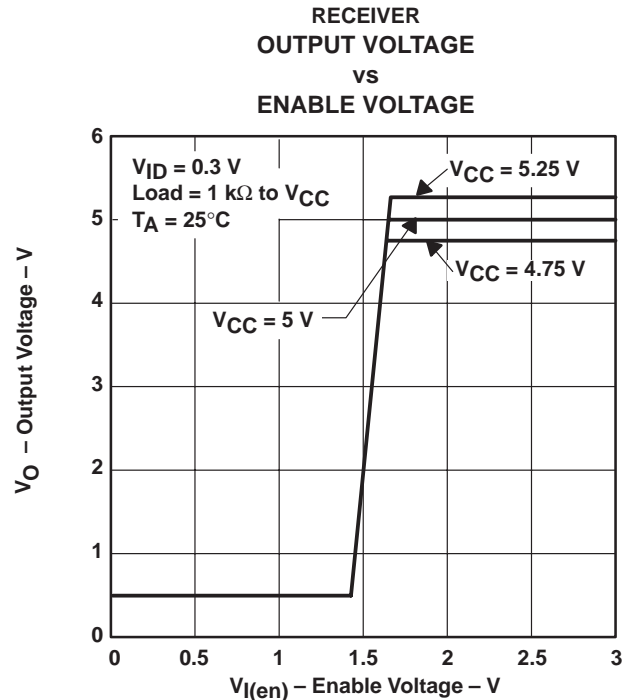
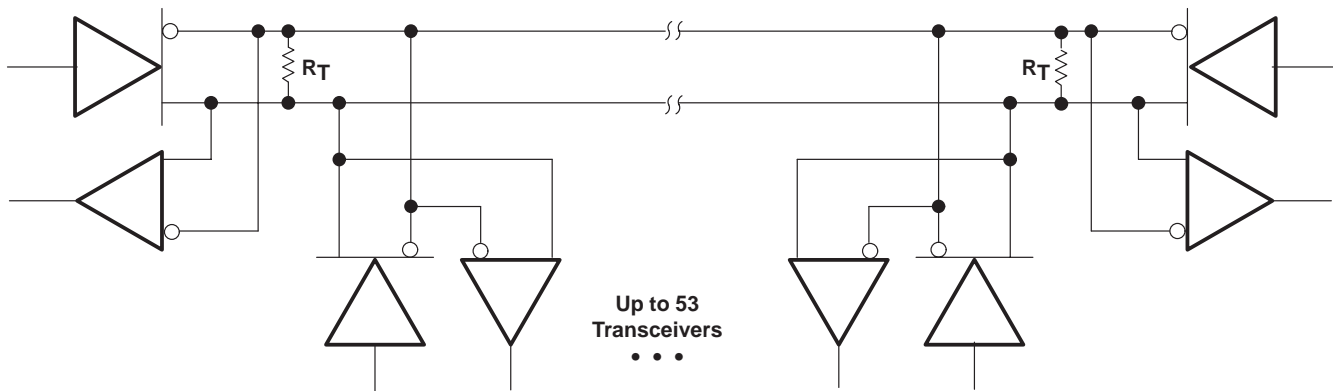


Figure 17

† Operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied.

APPLICATION INFORMATION



NOTE A: The line should terminate at both ends in its characteristic impedance ($R_T = Z_0$). Stub lengths off the main line should be kept as short as possible.

Figure 18. Typical Application Circuit

IMPORTANT NOTICE

Texas Instruments and its subsidiaries (TI) reserve the right to make changes to their products or to discontinue any product or service without notice, and advise customers to obtain the latest version of relevant information to verify, before placing orders, that information being relied on is current and complete. All products are sold subject to the terms and conditions of sale supplied at the time of order acknowledgement, including those pertaining to warranty, patent infringement, and limitation of liability.

TI warrants performance of its semiconductor products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

CERTAIN APPLICATIONS USING SEMICONDUCTOR PRODUCTS MAY INVOLVE POTENTIAL RISKS OF DEATH, PERSONAL INJURY, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE ("CRITICAL APPLICATIONS"). TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS. INCLUSION OF TI PRODUCTS IN SUCH APPLICATIONS IS UNDERSTOOD TO BE FULLY AT THE CUSTOMER'S RISK.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards must be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance or customer product design. TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used. TI's publication of information regarding any third party's products or services does not constitute TI's approval, warranty or endorsement thereof.